

[METHOD AND CIRCUIT FOR PRECISE TIMING OF SIGNALS IN AN EMBEDDED DRAM ARRAY]

Abstract

A method and circuit for timing the start of a precharge period in an eDRAM. The circuit including: a delayed lock loop circuit for receiving a clock signal and generating a control signal for adjusting an internal delay of the clock signal; and means for generating a delayed clock signal in response to the control signal. The means for generating the delayed clock signal is a multiple stage delay circuit, each stage of the multiple delay stage circuit connected in series and each stage individually responsive to the control signal.